What is claimed is:

1. A method for identifying defects in an integrated circuit, comprising the steps of:

measuring a current signature delta value of a device under test; and

comparing the current signature delta value to a threshold current signature delta value to determine whether the current signature delta value is greater than the threshold current signature delta value.

2. The method according to claim 1, further comprising the step of generating the threshold current signature delta value for a statistically valid number of acceptable integrated circuits.

3. The method according to claim 2, wherein the step of generating the threshold current signature delta value that correlates to the acceptable integrated circuit further comprises the steps of:

applying a set of vectors to a statistically valid number of acceptable integrated circuits;

formulating a threshold base current signature for the statistically valid number of acceptable integrated circuits;

administering a voltage stress for a time period to each of the statistically valid number of acceptable integrated circuits;

applying the set of vectors to the statistically valid number of acceptable integrated circuits;

formulating a threshold post-stress current signature for the statistically valid number of acceptable integrated circuits;

comparing the threshold base current signature for the statistically valid number of acceptable integrated circuits to the threshold post-stress current signatures for the statistically valid number of acceptable integrated circuits to determine a threshold current signature delta value corresponding to an acceptable integrated circuit.

4. The method according to claim 1, further comprising the step of generating the threshold current signature delta value using a computer.

5. The method according to claim 3, wherein the step of measuring the current signature delta value of the device under test further comprises the steps of:

applying a set of vectors to the device under test and formulating a base current signature for the device under test;

administering a voltage stress to the device under test for a time period;

applying the set of vectors to the device under test and formulating a post-voltage stress current signature for the device under test; and

determining the current signature delta value for the device under test.

6. The method according to claim 4, wherein the step of measuring the current signature delta value of the device under test further comprises the steps of:

applying a set of vectors to the device under test and formulating a base current signature for the device under test;

administering a voltage stress to the device under test for a time period;

applying the set of vectors to the device under test and formulating a post-voltage stress current signature for the device under test; and

determining the current signature delta value for the device under test.

7. The method according to claim 5, further comprising the step of:

comparing the post-voltage stress current signature of the device under test to the threshold post-voltage stress current signature to determine whether the post-voltage stress current signature of the device under test is greater.

8. The method according to claim 6, further comprising the step of:

comparing the post-voltage stress current signature of the device under test to the threshold post-voltage stress current signature to determine whether the post-voltage stress current signature of the device under test is greater.

9. The method according to claim 7, wherein the threshold current signature delta value is equivalent to a largest difference between the threshold post-voltage stress current signature and the threshold base current signature for the statistically valid number of acceptable integrated circuits.

10. The method according to claim 8, wherein the current signature delta value for the device under test is a difference between the post-voltage stress current signature and the base current signature of the device under test.

11. The method according to claim 9, wherein the current signature delta value for the device under test is a difference between the post-voltage stress current signature and the base current signature of the device under test.

12. The method according to claim 11, wherein said formulating the threshold base current signature for the statistically valid number of acceptable integrated circuits further comprises the steps of:

measuring a base current response for each vector of a set of measured vectors from the set of vectors applied to each of the statistically valid number of acceptable integrated circuits;

determining the lowest base current response for each vector as applied across each of the statistically valid number of acceptable integrated circuits; and

plotting the lowest base current responses for the set of vectors into the threshold base current signature.

13. The method according to claim 12, wherein said formulating the threshold post-voltage stress current signature for the statistically valid number of acceptable integrated circuits further comprises the steps of:

measuring a post-voltage stress current response for each vector of a set of measured vectors from the set of vectors applied across each of the statistically valid number of acceptable integrated circuits;

determining the highest post-voltage stress current response for each vector as applied across each of the experimental ICs; and

plotting the highest post-voltage stress current responses for the set of vectors into the threshold post-voltage stress current signature.

14. The method according to claim 13, wherein said formulating the base current signature for the device under test comprises the step of measuring a current response for each vector of the set of measured vectors applied to the device under test and plotting the current response for each vector of the set of measured vectors into the base current signature for the device under test.

15. The method according to claim 14, wherein said formulating the post-voltage stress current signature for the device under test comprises the step of measuring a post-voltage stress current response for each vector of the set of measured vectors applied to the device under test after said administering the voltage stress for the time period, and plotting the post-voltage stress current response for each vector of into the post-voltage stress current signature for the device under test.

16. The method according to claim 15, wherein the statistically valid number of acceptable integrated circuits must have the same architecture as the device under test.

17. The method according to claim 16, wherein the statistically valid number of acceptable integrated circuits must be produced using the same semiconductor wafer process technology as the device under test.

18. The method according to claim 17, wherein the threshold base current signature and the threshold post-voltage stress current signature for the statistically valid number of acceptable integrated circuits are threshold base quiescent current signatures and threshold post-stress quiescent current signatures.

19. The method according to claim 18, wherein the threshold base current signature and the threshold post-voltage stress current signature for the device under test is a threshold base quiescent current signature and a threshold post-voltage stress quiescent current signature.

20. The method according to claim 19, wherein after said applying the set of vectors to the statistically valid number of acceptable integrated circuits and prior to said formulating the threshold base quiescent current signature for the statistically valid number of acceptable integrated circuits, each of the statistically valid number of acceptable integrated circuits are allowed to reach a steady state before the current measurement is recorded.

21. The method according to claim 20, wherein after said administering the voltage stress, after said applying the set of vectors to the statistically valid number of acceptable integrated circuits and prior to said formulating the threshold post-voltage stress quiescent current signature for the statistically valid number of acceptable integrated circuits, the statistically valid number of acceptable integrated circuits are allowed to reach a steady state before the current measurement is recorded.

22. The method according to claim 21, wherein after said applying the set of vectors to the device under test and prior to said formulating the base current signature for the device

under test, the device under test is be allowed to reach steady state before each current measurement is recorded.

23. The method according to claim 22, wherein after said administering the voltage stress, after said applying the set of vectors to the device under test and prior to said formulating the post-voltage stress current signature for the device under test, the device under test is allowed to reach steady state before each current measurement is recorded.

24. The method according to claim 17, wherein the base current signatures and the post-stress current signatures for each of the statistically valid number of acceptable integrated circuits are base transient current signatures and post-stress transient current signatures.

25. The method according to claim 24, wherein the base current signature and the post-voltage stress current signature for the device under test is a base transient current signature and a post-stress transient current signature.

26. The method according to claim 23, wherein the set of vectors is generated using an automatic test generation program.

27. The method according to claim 26, wherein said applying a set of vectors to the device under test and the statistically valid number of acceptable integrated circuits is performed using a VLSI test system.

28. The method according to claim 27, wherein said measuring the current signature delta value of the device under test and the statistically valid number of acceptable integrated circuits is performed using the VLSI test system.

29. The method according to claim 28, wherein the set of vectors comprises less than one hundred vectors.

30. The method according to claim 29, wherein the set of vectors comprises vectors associated with a high fault coverage for the device under test.

31. The method according to claim 30, wherein the set of vectors comprises vectors associated with low current off-states for the device under test.

32. The method according to claim 31, wherein the time period for said administering the voltage stress to the statistically valid number of acceptable integrated circuits and to the device under test is equivalent to the minimum amount of time that the voltage stress can be administered to an acceptable integrated circuit in which the acceptable integrated circuit remains acceptable.

33. An apparatus for identifying defects in an integrated circuit, comprising:

a generator for generating a set of vectors for applying to a device under test;

a measurer for measuring a current signature delta value of the device under test; and

a comparing means for comparing the current signature delta value to an experimental threshold current signature delta value to determine whether the current signature delta value is greater than the threshold current signature delta value.

34. The apparatus according to claim 33, wherein the measurer measures the experimental threshold current signature delta value for the statistically valid number of acceptable integrated circuits by:

applying a set of vectors to the statistically valid number of acceptable integrated circuits;

formulating a threshold base current signature for the statistically valid number of acceptable integrated circuits from the set of measured vectors;

administering a voltage stress for a time period to the statistically valid number of acceptable integrated circuits;

applying the set of vectors to the statistically valid number of acceptable integrated circuits;

formulating a threshold post-stress current signature for the statistically valid number of acceptable integrated circuits from the set of measured vectors; and

comparing the threshold base current signature for the statistically valid number of acceptable integrated circuits to the threshold post-stress current signatures for the statistically valid number of acceptable integrated circuits to determine a threshold current signature delta value corresponding to an acceptable integrated circuit.

35. The apparatus according to claim 33, further comprising a computer for computing the experimental threshold current signature delta value.

36. The apparatus according to claim 33, wherein the generator generates a set of measured vectors from the set of vectors for applying to the device under test.

37. The apparatus according to claim 35, wherein the measurer measures the current signature delta value of the device under test by:

applying a set of vectors to the device under test;

formulating a base current signature for the device under test from the set of measured vectors;

administering a voltage stress for a time period to the device under test;

applying the set of vectors to the device under test;

formulating a threshold post-stress current signature for the device under test from the set of measured vectors;

comparing the base current signature for the device under test to the post-stress current signatures for the device under test to determine a the current signature delta value for the device under test.

38. The apparatus according to claim 36, wherein the measurer measures the current signature delta value of the device under test by:

applying a set of vectors to the device under test;

formulating a base current signature for the device under test from the set of measured vectors;

administering a voltage stress for a time period to the device under test;

applying the set of vectors to the device under test;

formulating a threshold post-stress current signature for the device under test from the set of measured vectors; and

comparing the base current signature for the device under test to the post-stress current signatures for the device under test to determine a the current signature delta value for the device under test.

39. The apparatus according to claim 37, wherein the threshold current signature delta value generated by the generator is equivalent to a largest difference between the post-voltage stress current signature and the base current signature of the statistically valid number of acceptable integrated circuits.

40. The apparatus according to claim 38, wherein the threshold current signature delta value generated by the generator is equivalent to a largest difference between the post-voltage stress current signature and the base current signature of the statistically valid number of acceptable integrated circuits.

41. The apparatus according to claim 39, wherein the current signature delta value for the device under test is a difference between the post-voltage stress current signature and the base current signature of the device under test.

42. The apparatus according to claim 41, wherein the generator generates the set of vectors for applying to a statistically valid number of acceptable integrated circuits; and the measurer measures the experimental threshold current signature delta value of the statistically valid number of acceptable integrated circuits.